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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/620,395 | 07/16/2003 | Yibing Zhao | Analog.7042 | 9544 |

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Attn: Matthew E. Connors
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| EXAMINER | |
|---|---|
| TRAN, ANH Q | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2819 | |

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/620,395 | ZHAO ET AL. | |
| | Examiner | Art Unit | |
| | Anh Q. Tran | 2819 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *13 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-17,19-42 and 45-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-21* is/are allowed.

6)☒ Claim(s) *1-16,22-33,35-38,40-42 and 45-47* is/are rejected.

7)☒ Claim(s) *17,34 and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 7 rejected under 35 U.S.C. 102(b) as being anticipated by Hamada et al (6,373,291).

Hamada shows:

1. A switch comprising:

a plurality of field effect transistors (PM0 and NM0, Fig. 4) connected in series, each field effect transistor including a gate, a source, and a drain, each gate having a gate width and a gate length;

said gate length of one of said series connected field effect transistors being a different size from said gate length of another series connected field effect transistor (col. 8, lines 9-14).

2. The switch as claimed in claim 1, wherein said gate of one of said plurality of series connected field effect transistor has a longer gate length (LPM0 is twice LNM0, (col. 8, lines 9-14) than said gate of said other series connected field effect transistor.

7. The switch as claimed in claim 1, wherein the different gate sizes increase a parasitic capacitance within the switch.

3. Claims 8, 9, 14-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Sun (4,890,077).

Sun shows:

8. a plurality of dual-gate field effect transistors (300 and 100, Fig. 13) connected in series, each dual-gate field effect transistor including two gates, a source, and a drain;

one of said series connected dual-gate field effect transistors having a modified gate therein that is of a different size from gates (col. 14, lines 20-25) of other series connected dual-gate field effect transistors.

9. The switch as claimed in claim 8, wherein said modified gate of said series connected dual-gate field effect transistor has a longer gate length and/or gate width (wider gate width, col. 14, lines 20-25), than gates of said other series connected dual-gate field effect transistor.

14. The switch as claimed in claim 8, wherein a second series (300', 200 and 200') connected dual-gate field effect transistor has a modified gate therein that is of a different size from gates of other series (300' is large size than 100) connected dual-gate field effect transistors.

15. The switch as claimed in claim 8, wherein said dual-gate field effect transistors are high-electron-mobility-transistors.

16. The switch as claimed in claim 8, wherein the different gate sizes increase a parasitic capacitance within the switch.

4. Claims 47 is rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al (5,514,992).

47. Tanaka show series connected dual-gate transistor (2A), comprising:

a first gate (G1); and

a second gate (G2);

said first gate having a gate width and a gate length;

said second gate having a gate width and a gate length;

said gate length of said first gate being a different size from said gate length of said second gate (col. 6, lines 37-39);

said gate width of said first gate being a different size (col. 6, lines 40-45) from said gate width of said second gate.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamada et al (6,373,291).

Hamada discloses the claimed invention except for:

-wherein said gate of one of said plurality of series connected field effect transistor has a distance to its drain port that is less than a distance to its source pod.

-wherein said gate of one of said plurality of series connected field effect transistor has a distance to its source port that is less than a distance to its drain port.

-wherein said gate of said other series connected field effect transistor has a distance to its source port that is equal to a distance to its drain port.

-wherein said gate of said other series connected field effect transistor has a distance to its source port that is equal to a distance to its drain port.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to adjust

-the gate of one of the plurality of series connected field effect transistor has a distance to its drain port that is less than a distance to its source port.

-the gate of one of the plurality of series connected field effect transistor has a distance to its source port that is less than a distance to its drain port.

-the gate of the other series connected field effect transistor has a distance to its source pod that is equal to a distance to its drain port.

-the gate of the other series connected field effect transistor has a distance to its source port that is equal to a distance to its drain port, since it has been held that the provision of adjustability, where needed, involves only routine skill in the art.

Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sun (4,890,077)

Sun discloses the claimed invention except for:

-wherein said gate of one of said series connected dual-gate field effect transistor has a distance to its drain port that is less than a distance to its source pod.

-wherein said gate of one of series connected dual-gate field effect transistor has a distance to its source port that is less than a distance to its drain port.

-wherein said gate of said other series connected dual-gate field effect transistor has a distance to its source port that is equal to a distance to its drain port.

-wherein said gate of said other series connected dual-gate field effect transistor has a distance to its source port that is equal to a distance to its drain port.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to adjust

-the gate of one of series connected dual-gate field effect transistor has a distance to its drain port that is less than a distance to its source port.

-the gate of one of series connected dual-gate field effect transistor has a distance to its source port that is less than a distance to its drain port.

-the gate of the other series connected dual-gate field effect transistor has a distance to its source pod that is equal to a distance to its drain port.

-the gate of the other series connected dual-gate field effect transistor has a distance to its source port that is equal to a distance to its drain port, since it has been held that the provision of adjustability, where needed, involves only routine skill in the art.

6. Claims 22-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kameyama et al (5,748,053) in view of Sun (4,890,077).

22. Kameyama discloses a radio frequency single pole double throw switch, comprising:

a receiver port (103, Fig. 2A); a transmitter port (102); an antenna port (101);

a receiver section connecting said receiver port to said antenna; and a transmitter section connecting said transmitter port to said antenna.

Kameyama discloses the claimed invention except for the receiver section including a plurality of dual-gate field effect transistors connected in series, each dual-gate field effect transistor including two gates, a source, and a drain such that one of said series connected dual-gate field effect transistors has a modified gate therein that is of a different size from gates of other series connected dual-gate field effect transistors.

However, Sun discloses a receiver section (Fig. 13) including a plurality of dual-gate field effect transistors connected in series (300 and 100), each dual-gate field effect transistor including two gates, a source, and a drain such that one of said series connected dual-gate field effect transistors has a modified gate therein that is of a different size (col. 14, lines 20-25) from gates of other series connected dual-gate field effect transistors.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the receiver section of Kameyama with the receiver of

Sun, in order to increased power dissipation without significant degradation of the FET performance at higher frequencies.

23. Sun shows a source of the modified gate transistor (300) is connected to the receiver port (22 or RF OUT).

24. The radio frequency single pole double throw switch as claimed in claim 22, wherein a drain (750) of said modified gate transistor is connected to said antenna port (20 or RF IN).

25. The radio frequency single pole double throw switch as claimed in claim 22, wherein a second series (300', 200, 200') connected dual-gate field effect transistor has a second modified gate therein that is of a different size (300' are larger than 100) from gates of other series connected dual-gate field effect transistors.

26. The radio frequency single pole double throw switch as claimed in claim 25, wherein a source (710) of said modified gate transistor is connected to said receiver port (22 or RF OUT) and a drain (connect by 300) of said second modified gate transistor is connected to said antenna port (20 or RF IN).

27. The radio frequency single pole double throw switch as claimed in claim 22, wherein said dual-gate field effect transistors are high-electron-mobility-transistors.

28. The radio frequency single pole double throw switch as claimed in claim 22, wherein said modified gate of said series connected dual-gate field effect transistor has a longer gate length and/or gate width (wider gate width) than gates of said other, series connected dual-gate field effect transistor.

33. wherein the different gate sizes increase a parasitic capacitance within the switch.

29-32. Kameyama in view of Sun above discloses the claimed invention except for:

-wherein said gate of one of said series connected dual-gate field effect transistor has a distance to its drain port that is less than a distance to its source pod.

-wherein said gate of one of series connected dual-gate field effect transistor has a distance to its source port that is less than a distance to its drain port.

-wherein said gate of said other series connected dual-gate field effect transistor has a distance to its source port that is equal to a distance to its drain port.

-wherein said gate of said other series connected dual-gate field effect transistor has a distance to its source port that is equal to a distance to its drain port.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to adjust

-the gate of one of series connected dual-gate field effect transistor has a distance to its drain port that is less than a distance to its source port.

-the gate of one of series connected dual-gate field effect transistor has a distance to its source port that is less than a distance to its drain port.

-the gate of the other series connected dual-gate field effect transistor has a distance to its source pod that is equal to a distance to its drain port.

-the gate of the other series connected dual-gate field effect transistor has a distance to its source port that is equal to a distance to its drain port, since it has been held that the provision of adjustability, where needed, involves only routine skill in the art.

7. Claims 35-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kameyama et al (5,748,053) in view of Sun (4,890,077) further view of Tanaka et al (5,514,992).

35. The combination of Kameyama and Sun, as described above in claims 22 with transistor 300 as a first receiver dual-gate transistor and transistor 100 as second receiver dual-gate transistor, discloses the claimed invention except for different length between the two transistors. However, Tanaka discloses two FET transistors connected in series having different gate lengths (Fig. 1C) to improve the breakdown voltage.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify transistor 300 and 100 of combination of Kameyama and Sun having different gate lengths, as taught by Tanaka in order to improve the breakdown voltage.

36-37. the limitations are rejected as above claims 23-24.

38. The radio fequency single pole double throw switch as claimed in claim 35, wherein said transmitter section includes a first transmitter dual-gate high electron mobility transistor having gates of different lengths and a second transmitter dual-gate high electron mobility transistor having gates of different lengths (replace the transmitter

section of Kameyama with another circuit, Fig. 13, of Sun which connected RF IN or 20 to the antenna port of Kameyama with 300 as a first transmitter dual-gate and 100 as a second transmitter dual-gate transistor).

40-42, 45. the limitations are rejected as above claims 27-28, and 29-33.

46. The radio frequency single pole double throw switch claimed in claim 35, wherein the different gate lengths improve the linearity without impacting the ESD and EOS ruggedness.

***Allowable Subject Matter***

8. Claims 17, 34, 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

17, 34. a heavily doped cap layer fabricated upon the transistor connection segment between the gates.

39. the source of the first transmitter dual-gate transistor is connected to the receiver port and the drain of the second transmitter dual-gate transistor is connected to the antenna port.

9. Claims 19-21 allowed.

10. The following is an examiner's statement of reasons for allowance: Although the prior art of record disclose dual-gate transistor with different width and length, with respect to claim 19, in addition to other limitations in the claims, the prior art of record fails to teach or disclose the applicant's invention as claimed, particularly the feature describing: a heavily doped cap layer fabricated upon the transistor connection segment between the gate finger.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

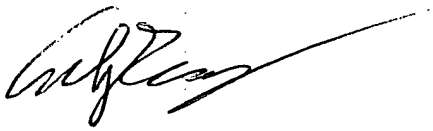
***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**ANH Q. TRAN**
**PRIMARY EXAMINER**



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